


# GA-990FXA-UD3

**Revision : 3.02**

PAGE	TITLE
01	COVER SHEET
02	BOM & PCB MODIFY HISTORY
03	BLOCK DIAGRAM
04	CPU HYPER TRANSPORT
05	CPU DDR3 MEMORY
06	CPU CONTROL
07	CPU POWER & GND
08	DDR3 CHANNEL A
09	DDR3 CHANNEL B
10	RD990 HT-LINK I/F, PCIE I/F
11	RD990 SYSTEM I/F, STRAPS
12	RD990 POWER & GND
13	ICS9LPRS477
14	ATI SB950 PCIE/PCI/CPU/LPC
15	ATI SB950 ACPI/USB/GPIO/AUDIO
16	ATI SB950 SATA/SPI/IDE/HWM
17	ATI SB950 POWER & GND
18	PCI EXPRESS x16 ,x1
19	PCI EXPRESS x16 ,X4
20	PCI SLOT , PCIEx4
21	ITE 8728EX ,Dual_BIOS ,HWM ,KB/MS
22	F_USB, IPWR
23	ALC889
24	AUDIO JACK
25	FAN/HWMO/COM

[illegible]

			
Title			
COVER SHEET			
Size	Document Number	Rev	
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**Model Name:GA-990FXA-UD3**

## Component value change history

4 Layer, 4mil 50ohm +/- 15% X

**Version: 3.02**


**P-Code:**  
**U98145-0**

[illegible]

**Circuit or PCB layout change for next version**

[illegible]

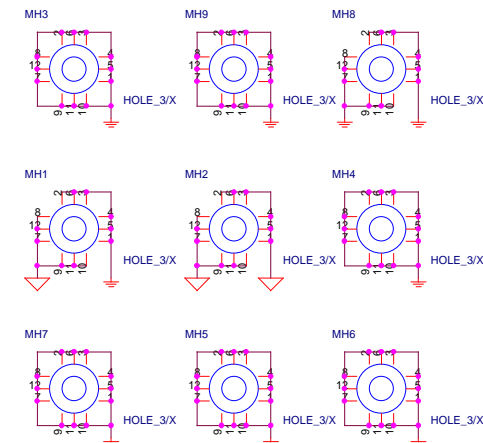
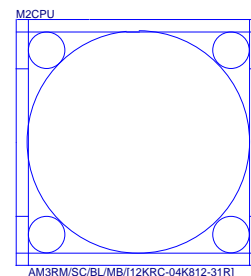
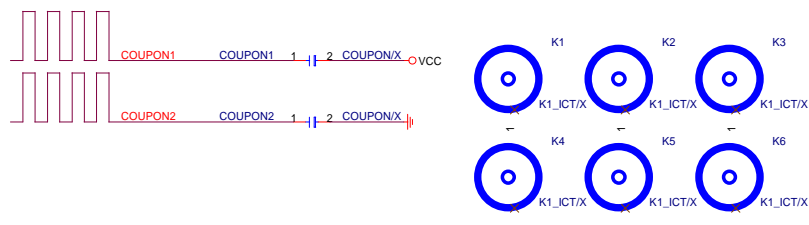
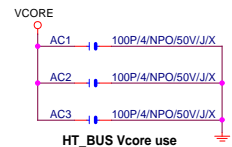
AM2-->AM3 Different: AE9-->AE7,  
H22-->H20. Extra pin: B2 AM3 socket is  
938 pins. Only shift 2 pins.

				
Title				
BOM & PCB HISTORY				
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```
CPU_VDD_RUN = VCORE
CPU_VDDA_RUN = VDDA25
VLDT_RUN = VCC12_HT
CPU_VDDIO_SUS = DDR15V
CPU_VDDR = CPU_VDDR12
```

```
VLDT_A = VCC12_HT
VLDT_B = HT12B
```





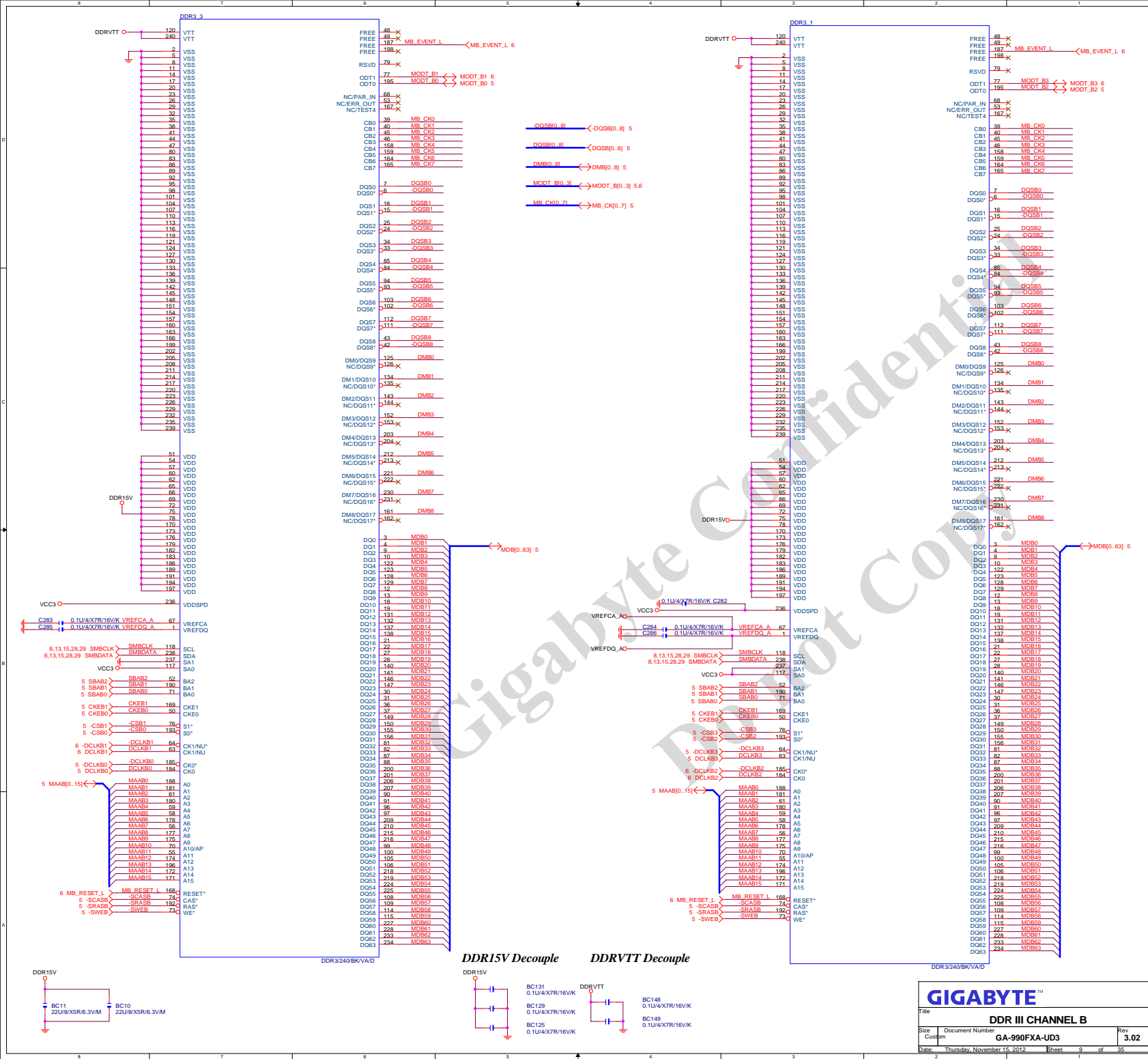






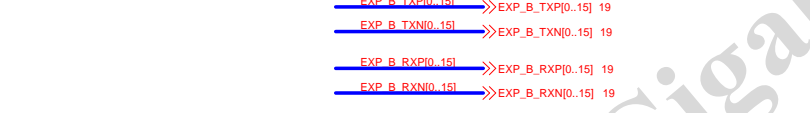
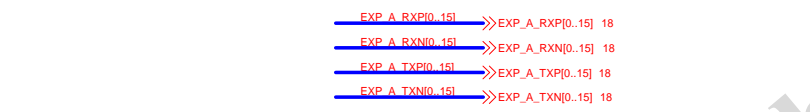
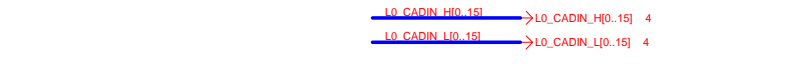




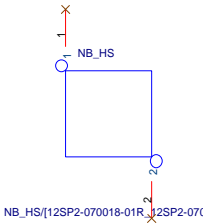


L0_CADOUT_H15	T25	HT_RXCAD15P	HT_TXCAD15P	N23	L0_CADIN_H15
L0_CADOUT_L15	T24	HT_RXCAD15N	HT_TXCAD15N	N24	L0_CADIN_L15
L0_CADOUT_H14	U24	HT_RXCAD14P	HT_TXCAD14P	M25	L0_CADIN_H14
L0_CADOUT_L14	U23	HT_RXCAD14N	HT_TXCAD14N	M24	L0_CADIN_L14
L0_CADOUT_H13	V25	HT_RXCAD13P	HT_TXCAD13P	L23	L0_CADIN_H13
L0_CADOUT_L13	V24	HT_RXCAD13N	HT_TXCAD13N	L24	L0_CADIN_L13
L0_CADOUT_H12	W24	HT_RXCAD12P	HT_TXCAD12P	K24	L0_CADIN_H12
L0_CADOUT_L12	W23	HT_RXCAD12N	HT_TXCAD12N	K25	L0_CADIN_L12
L0_CADOUT_H11	AA24	HT_RXCAD11P	HT_TXCAD11P	H24	L0_CADIN_H11
L0_CADOUT_L11	AA23	HT_RXCAD11N	HT_TXCAD11N	H25	L0_CADIN_L11
L0_CADOUT_H10	AB25	HT_RXCAD10P	HT_TXCAD10P	G23	L0_CADIN_H10
L0_CADOUT_L10	AB24	HT_RXCAD10N	HT_TXCAD10N	G24	L0_CADIN_L10
L0_CADOUT_H9	AC24	HT_RXCAD9P	HT_TXCAD9P	F24	L0_CADIN_H9
L0_CADOUT_L9	AC23	HT_RXCAD9N	HT_TXCAD9N	F25	L0_CADIN_L9
L0_CADOUT_H8	AD25	HT_RXCAD8P	HT_TXCAD8P	E23	L0_CADIN_H8
L0_CADOUT_L8	AD24	HT_RXCAD8N	HT_TXCAD8N	E24	L0_CADIN_L8
L0_CADOUT_H7	T28	HT_RXCAD7P	HT_TXCAD7P	N26	L0_CADIN_H7
L0_CADOUT_L7	T27	HT_RXCAD7N	HT_TXCAD7N	M27	L0_CADIN_L7
L0_CADOUT_H6	U27	HT_RXCAD6P	HT_TXCAD6P	M28	L0_CADIN_H6
L0_CADOUT_L6	U26	HT_RXCAD6N	HT_TXCAD6N	L26	L0_CADIN_L6
L0_CADOUT_H5	V28	HT_RXCAD5P	HT_TXCAD5P	L27	L0_CADIN_H5
L0_CADOUT_L5	V27	HT_RXCAD5N	HT_TXCAD5N	K27	L0_CADIN_L5
L0_CADOUT_H4	W27	HT_RXCAD4P	HT_TXCAD4P	K28	L0_CADIN_H4
L0_CADOUT_L4	W26	HT_RXCAD4N	HT_TXCAD4N	J28	L0_CADIN_L4
L0_CADOUT_H3	AA27	HT_RXCAD3P	HT_TXCAD3P	G28	L0_CADIN_H3
L0_CADOUT_L3	AA26	HT_RXCAD3N	HT_TXCAD3N	G29	L0_CADIN_L3
L0_CADOUT_H2	AB28	HT_RXCAD2P	HT_TXCAD2P	G26	L0_CADIN_H2
L0_CADOUT_L2	AB27	HT_RXCAD2N	HT_TXCAD2N	G27	L0_CADIN_L2
L0_CADOUT_H1	AC27	HT_RXCAD1P	HT_TXCAD1P	F28	L0_CADIN_H1
L0_CADOUT_L1	AC26	HT_RXCAD1N	HT_TXCAD1N	E28	L0_CADIN_L1
L0_CADOUT_H0	AD28	HT_RXCAD0P	HT_TXCAD0P	E26	L0_CADIN_H0
L0_CADOUT_L0	AD27	HT_RXCAD0N	HT_TXCAD0N	E27	L0_CADIN_L0

4 L0_CLKOUT_H1	L0_CLKOUT_H1	Y25	HT_RXCLK1P	HT_TXCLK1P	J23	L0_CLKIN_H1	L0_CLKIN_H1	4
4 L0_CLKOUT_L1	L0_CLKOUT_L1	Y24	HT_RXCLK1N	HT_TXCLK1N	J24	L0_CLKIN_L1	L0_CLKIN_L1	4
4 L0_CLKOUT_H0	L0_CLKOUT_H0	Y28	HT_RXCLK0P	HT_TXCLK0P	J26	L0_CLKIN_H0	L0_CLKIN_H0	4
4 L0_CLKOUT_L0	L0_CLKOUT_L0	Y27	HT_RXCLK0N	HT_TXCLK0N	J27	L0_CLKIN_L0	L0_CLKIN_L0	4
4 L0_CTOUT_H1	L0_CTOUT_H1	R24	HT_RXCTL1P	HT_TXCTL1P	P24	L0_CTIN_H1	L0_CTIN_H1	4
4 L0_CTOUT_L1	L0_CTOUT_L1	R23	HT_RXCTL1N	HT_TXCTL1N	P25	L0_CTIN_L1	L0_CTIN_L1	4
4 L0_CTOUT_H0	L0_CTOUT_H0	R27	HT_RXCTL0P	HT_TXCTL0P	P28	L0_CTIN_H0	L0_CTIN_H0	4
4 L0_CTOUT_L0	L0_CTOUT_L0	R26	HT_RXCTL0N	HT_TXCTL0N	P27	L0_CTIN_L0	L0_CTIN_L0	4



N.B HEATSINK

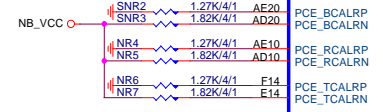
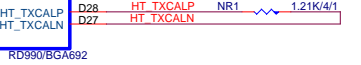


PART 1/5

HYPERTRANSPORT  
IF

HT_TXCAD15P	N23	L0_CADIN_H15
HT_TXCAD15N	N24	L0_CADIN_L15
HT_TXCAD14P	M25	L0_CADIN_H14
HT_TXCAD14N	M24	L0_CADIN_L14
HT_TXCAD13P	L23	L0_CADIN_H13
HT_TXCAD13N	L24	L0_CADIN_L13
HT_TXCAD12P	K24	L0_CADIN_H12
HT_TXCAD12N	K25	L0_CADIN_L12
HT_TXCAD11P	H24	L0_CADIN_H11
HT_TXCAD11N	H25	L0_CADIN_L11
HT_TXCAD10P	G23	L0_CADIN_H10
HT_TXCAD10N	G24	L0_CADIN_L10
HT_TXCAD9P	F24	L0_CADIN_H9
HT_TXCAD9N	F25	L0_CADIN_L9
HT_TXCAD8P	E23	L0_CADIN_H8
HT_TXCAD8N	E24	L0_CADIN_L8
HT_TXCAD7P	N26	L0_CADIN_H7
HT_TXCAD7N	M27	L0_CADIN_L7
HT_TXCAD6P	M28	L0_CADIN_H6
HT_TXCAD6N	L26	L0_CADIN_L6
HT_TXCAD5P	L27	L0_CADIN_H5
HT_TXCAD5N	K27	L0_CADIN_L5
HT_TXCAD4P	K28	L0_CADIN_H4
HT_TXCAD4N	J28	L0_CADIN_L4
HT_TXCAD3P	G28	L0_CADIN_H3
HT_TXCAD3N	G29	L0_CADIN_L3
HT_TXCAD2P	G26	L0_CADIN_H2
HT_TXCAD2N	G27	L0_CADIN_L2
HT_TXCAD1P	F28	L0_CADIN_H1
HT_TXCAD1N	E28	L0_CADIN_L1
HT_TXCAD0P	E26	L0_CADIN_H0
HT_TXCAD0N	E27	L0_CADIN_L0

HT_RXCLK1P	J23	L0_CLKIN_H1	L0_CLKIN_H1	4
HT_RXCLK1N	J24	L0_CLKIN_L1	L0_CLKIN_L1	4
HT_RXCLK0P	J26	L0_CLKIN_H0	L0_CLKIN_H0	4
HT_RXCLK0N	J27	L0_CLKIN_L0	L0_CLKIN_L0	4
HT_RXCTL1P	P24	L0_CTIN_H1	L0_CTIN_H1	4
HT_RXCTL1N	P25	L0_CTIN_L1	L0_CTIN_L1	4
HT_RXCTL0P	P28	L0_CTIN_H0	L0_CTIN_H0	4
HT_RXCTL0N	P27	L0_CTIN_L0	L0_CTIN_L0	4



PART 2/5

PCIe  
GPP1

PCIe  
GPP2

PCIe  
ALINK

EXP_A_RXP15	N6	GPP1_RX15P
EXP_A_RXN15	N5	GPP1_RX15N
EXP_A_RXP14	M5	GPP1_RX14P
EXP_A_RXN14	M4	GPP1_RX14N
EXP_A_RXP13	L5	GPP1_RX13P
EXP_A_RXN13	L4	GPP1_RX13N
EXP_A_RXP12	K5	GPP1_RX12P
EXP_A_RXN12	K4	GPP1_RX12N
EXP_A_RXP11	J5	GPP1_RX11P
EXP_A_RXN11	J4	GPP1_RX11N
EXP_A_RXP10	H5	GPP1_RX10P
EXP_A_RXN10	H4	GPP1_RX10N
EXP_A_RXP9	G6	GPP1_RX9P
EXP_A_RXN9	G5	GPP1_RX9N
EXP_A_RXP8	F6	GPP1_RX8P
EXP_A_RXN8	F5	GPP1_RX8N
EXP_A_RXP7	D2	GPP1_RX7P
EXP_A_RXN7	D1	GPP1_RX7N
EXP_A_RXP6	B6	GPP1_RX6P
EXP_A_RXN6	B5	GPP1_RX6N
EXP_A_RXP5	A6	GPP1_RX5P
EXP_A_RXN5	A5	GPP1_RX5N
EXP_A_RXP4	E7	GPP1_RX4P
EXP_A_RXN4	E6	GPP1_RX4N
EXP_A_RXP3	D7	GPP1_RX3P
EXP_A_RXN3	D6	GPP1_RX3N
EXP_A_RXP2	E8	GPP1_RX2P
EXP_A_RXN2	E7	GPP1_RX2N
EXP_A_RXP1	E9	GPP1_RX1P
EXP_A_RXN1	E8	GPP1_RX1N
EXP_A_RXP0	E10	GPP1_RX0P
EXP_A_RXN0	E9	GPP1_RX0N

EXP_B_RXP15	AC9	GPP2_RX15P
EXP_B_RXN15	AD9	GPP2_RX15N
EXP_B_RXP14	AE8	GPP2_RX14P
EXP_B_RXN14	AE7	GPP2_RX14N
EXP_B_RXP13	AC7	GPP2_RX13P
EXP_B_RXN13	AD7	GPP2_RX13N
EXP_B_RXP12	AE6	GPP2_RX12P
EXP_B_RXN12	AE5	GPP2_RX12N
EXP_B_RXP11	AE5	GPP2_RX11P
EXP_B_RXN11	AE6	GPP2_RX11N
EXP_B_RXP10	AE2	GPP2_RX10P
EXP_B_RXN10	AE1	GPP2_RX10N
EXP_B_RXP9	AD2	GPP2_RX9P
EXP_B_RXN9	AD1	GPP2_RX9N
EXP_B_RXP8	AB5	GPP2_RX8P
EXP_B_RXN8	AB4	GPP2_RX8N
EXP_B_RXP7	AA6	GPP2_RX7P
EXP_B_RXN7	AA5	GPP2_RX7N
EXP_B_RXP6	Y5	GPP2_RX6P
EXP_B_RXN6	Y4	GPP2_RX6N
EXP_B_RXP5	W6	GPP2_RX5P
EXP_B_RXN5	W5	GPP2_RX5N
EXP_B_RXP4	V5	GPP2_RX4P
EXP_B_RXN4	V4	GPP2_RX4N
EXP_B_RXP3	U6	GPP2_RX3P
EXP_B_RXN3	U5	GPP2_RX3N
EXP_B_RXP2	T5	GPP2_RX2P
EXP_B_RXN2	T4	GPP2_RX2N
EXP_B_RXP1	R6	GPP2_RX1P
EXP_B_RXN1	R5	GPP2_RX1N
EXP_B_RXP0	P4	GPP2_RX0P
EXP_B_RXN0	P5	GPP2_RX0N

20_PCIE4_4P	AD11	GPP3_RX9P
20_PCIE4_4N	AD11	GPP3_RX9N
20_PCIE4_3P	AD12	GPP3_RX8P
20_PCIE4_3N	AD12	GPP3_RX8N
20_PCIE4_2P	AD13	GPP3_RX7P
20_PCIE4_2N	AD13	GPP3_RX7N
20_PCIE4_1P	AD14	GPP3_RX6P
20_PCIE4_1N	AD14	GPP3_RX6N
32_RB_SL_IP	AD15	GPP3_RX5P
32_RB_SL_IN	AD15	GPP3_RX5N
33_UB_USB3_IP	AD16	GPP3_RX4P
33_UB_USB3_IN	AD16	GPP3_RX4N
19_PCIE4_4P_SB	AD17	GPP3_RX3P
19_PCIE4_4N_SB	AD17	GPP3_RX3N
19_PCIE4_3P_SB	AD18	GPP3_RX2P
19_PCIE4_3N_SB	AD18	GPP3_RX2N
19_PCIE4_2P_SB	AD19	GPP3_RX1P
19_PCIE4_2N_SB	AD19	GPP3_RX1N
19_PCIE4_1P_SB	AD20	GPP3_RX0P
19_PCIE4_1N_SB	AD20	GPP3_RX0N

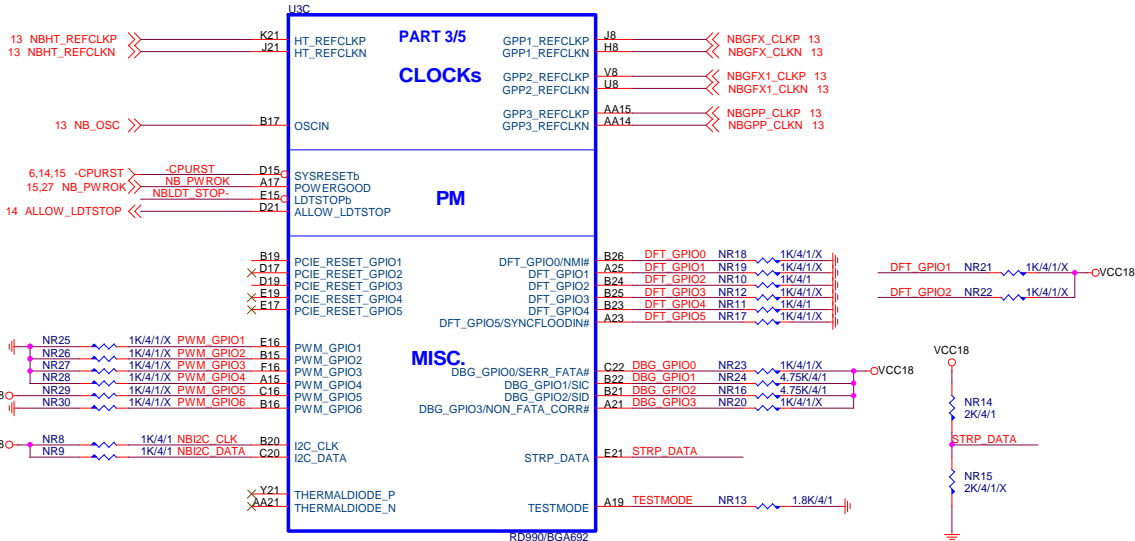
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14_A_RX3N	AC22	SB_RX3N
14_A_RX2P	AC23	SB_RX2P
14_A_RX2N	AC24	SB_RX2N
14_A_RX1P	AC25	SB_RX1P
14_A_RX1N	AC26	SB_RX1N
14_A_RX0P	AC27	SB_RX0P
14_A_RX0N	AC28	SB_RX0N

PCE_BCALRP	AE20	1.27K/4/1	SNR2
PCE_BCALRN	AD20	1.82K/4/1	SNR3
PCE_RCALRP	AE10	1.27K/4/1	NR4
PCE_RCALRN	AD10	1.82K/4/1	NR5
PCE_TCALRP	F14	1.27K/4/1	NR6
PCE_TCALRN	E14	1.82K/4/1	NR7

GPP1_TX15P	N3	EXP_A_TXP15
GPP1_TX15N	N2	EXP_A_TXN15
GPP1_TX14P	M2	EXP_A_TXP14
GPP1_TX14N	M1	EXP_A_TXN14
GPP1_TX13P	L3	EXP_A_TXP13
GPP1_TX13N	L2	EXP_A_TXN13
GPP1_TX12P	K2	EXP_A_TXP12
GPP1_TX12N	K1	EXP_A_TXN12
GPP1_TX11P	J3	EXP_A_TXP11
GPP1_TX11N	J2	EXP_A_TXN11
GPP1_TX10P	H3	EXP_A_TXP10
GPP1_TX10N	H2	EXP_A_TXN10
GPP1_TX9P	G3	EXP_A_TXP9
GPP1_TX9N	G2	EXP_A_TXN9
GPP1_TX8P	F2	EXP_A_TXP8
GPP1_TX8N	F1	EXP_A_TXN8
GPP1_TX7P	E3	EXP_A_TXP7
GPP1_TX7N	E2	EXP_A_TXN7
GPP1_TX6P	A4	EXP_A_TXP6
GPP1_TX6N	A3	EXP_A_TXN6
GPP1_TX5P	A6	EXP_A_TXP5
GPP1_TX5N	A5	EXP_A_TXN5
GPP1_TX4P	B7	EXP_A_TXP4
GPP1_TX4N	B6	EXP_A_TXN4
GPP1_TX3P	C7	EXP_A_TXP3
GPP1_TX3N	C6	EXP_A_TXN3
GPP1_TX2P	B8	EXP_A_TXP2
GPP1_TX2N	B7	EXP_A_TXN2
GPP1_TX1P	A10	EXP_A_TXP1
GPP1_TX1N	A9	EXP_A_TXN1
GPP1_TX0P	B11	EXP_A_TXP0
GPP1_TX0N	B10	EXP_A_TXN0

GPP2_TX15P	AF9	EXP_B_TXP15
GPP2_TX15N	AG9	EXP_B_TXN15
GPP2_TX14P	AG8	EXP_B_TXP14
GPP2_TX14N	AH8	EXP_B_TXN14
GPP2_TX13P	AF7	EXP_B_TXP13
GPP2_TX13N	AG7	EXP_B_TXN13
GPP2_TX12P	AG6	EXP_B_TXP12
GPP2_TX12N	AH6	EXP_B_TXN12
GPP2_TX11P	AG4	EXP_B_TXP11
GPP2_TX11N	AH4	EXP_B_TXN11
GPP2_TX10P	AE3	EXP_B_TXP10
GPP2_TX10N	AE2	EXP_B_TXN10
GPP2_TX9P	AC3	EXP_B_TXP9
GPP2_TX9N	AC2	EXP_B_TXN9
GPP2_TX8P	AB2	EXP_B_TXP8
GPP2_TX8N	AB1	EXP_B_TXN8
GPP2_TX7P	AA3	EXP_B_TXP7
GPP2_TX7N	AA2	EXP_B_TXN7
GPP2_TX6P	Y2	EXP_B_TXP6
GPP2_TX6N	Y1	EXP_B_TXN6
GPP2_TX5P	W3	EXP_B_TXP5
GPP2_TX5N	W2	EXP_B_TXN5
GPP2_TX4P	V2	EXP_B_TXP4
GPP2_TX4N	V1	EXP_B_TXN4
GPP2_TX3P	U2	EXP_B_TXP3
GPP2_TX3N	T2	EXP_B_TXN3
GPP2_TX2P	T1	EXP_B_TXP2
GPP2_TX2N	R3	EXP_B_TXP1
GPP2_TX1P	R2	EXP_B_TXP0
GPP2_TX1N	P2	EXP_B_TXN0
GPP2_TX0P	P1	EXP_B_TXN0

GPP3_TX9P	AH10	GPP_TX9P_C	C6
GPP3_TX9N	AG10	GPP_TX9N_C	C5
GPP3_TX8P	AG11	GPP_TX8P_C	C7
GPP3_TX8N	AF11	GPP_TX8N_C	C8
GPP3_TX7P	AH12	GPP_TX7P_C	C11
GPP3_TX7N	AG12	GPP_TX7N_C	C12
GPP3_TX6P	AG13	GPP_TX6P_C	C14
GPP3_TX6N	AF13	GPP_TX6N_C	C15
GPP3_TX5P	AH14	GPP_TX5P_C	NC4
GPP3_TX5N	AG14	GPP_TX5N_C	NC3
GPP3_TX4P	AG15	GPP_TX4P_C	NC6
GPP3_TX4N	AF15	GPP_TX4N_C	NC5
GPP3_TX3P	AH16	GPP_TX3P_C	NC7
GPP3_TX3N	AG16	GPP_TX3N_C	NC8
GPP3_TX2P	AG17	GPP_TX2P_C	NC10
GPP3_TX2N	AF17	GPP_TX2N_C	NC9
GPP3_TX1P	AH18	GPP_TX1P_C	NC10
GPP3_TX1N	AG19	GPP_TX1P_C	NC2
GPP3_TX0P	AF19	GPP_TX0N_C	NC1
GPP3_TX0N			



#### DFT\_GPIO5: STRAP\_DEBUG\_BUS\_GPIO\_ENABLEb

Enables the Test Debug Bus using GPIO.  
1 : Disable ( Can still be enabled using nbcfg register access)  
0 : Enable

#### DFT\_GPIO[4:2]: STRAP\_PCIE\_GPP\_CFG[2:0]

These pin straps are used to configure PCI-E GPP mode.  
GPIO4:3:2  
000 : 4:2:4 B  
001 : 4:1:1:4 C  
010 : 1:1:1:1:1:1:4 L (Hardware Default)  
011 : 2:1:1:1:1:1:4 E  
100 : 2:2:1:1:4 K  
101 : 2:2:2:4 C2  
110 : Hardware default (mode L) or EEPROM  
111 : Hardware default (mode L) or EEPROM  
101 : 01100  
111 : 01011

#### DFT\_GPIO1: LOAD\_EEPROM\_STRAPS

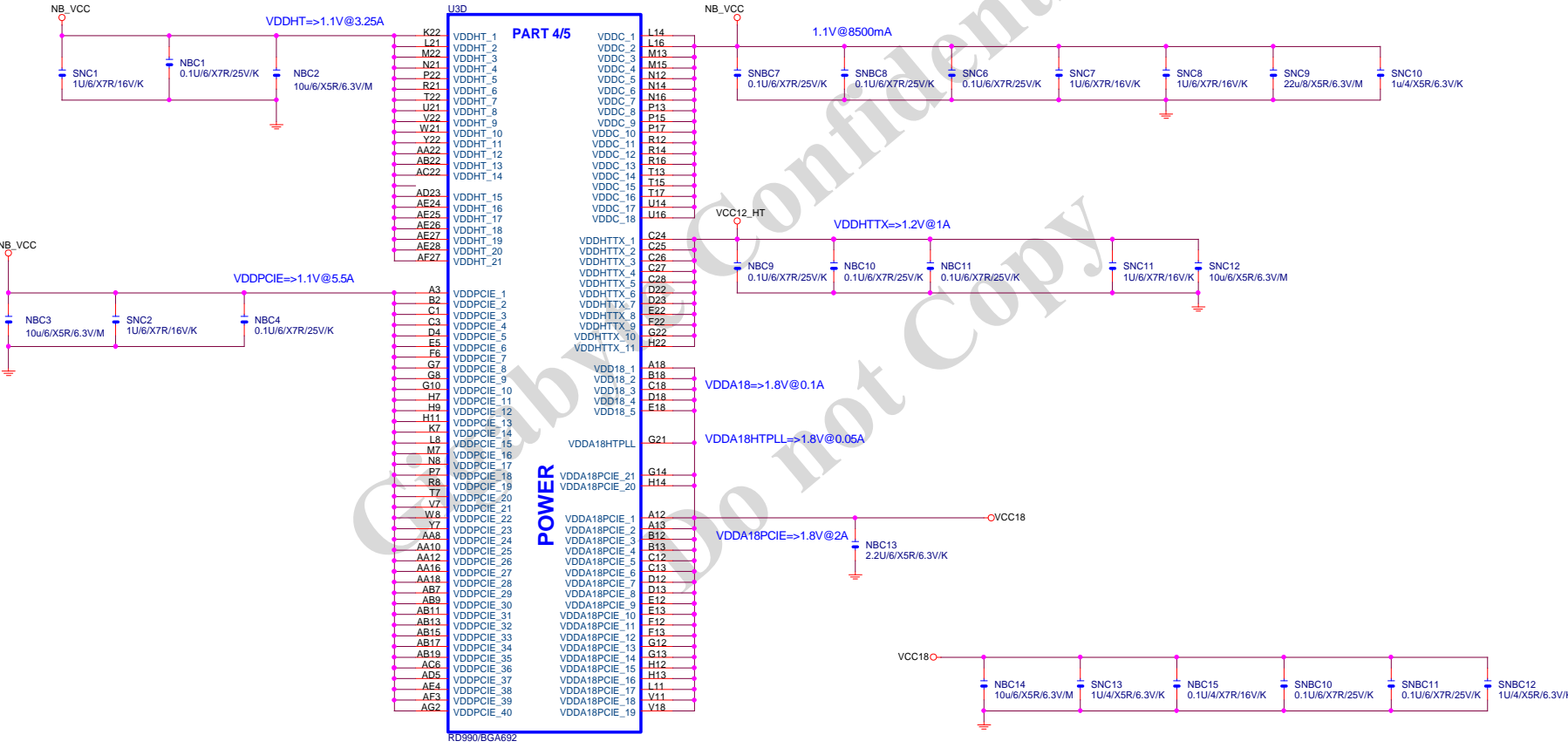
Selects Loading of STRAPS from EPROM  
1 : Bypass the loading of EEPROM straps and use Hardware Default Values  
0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected

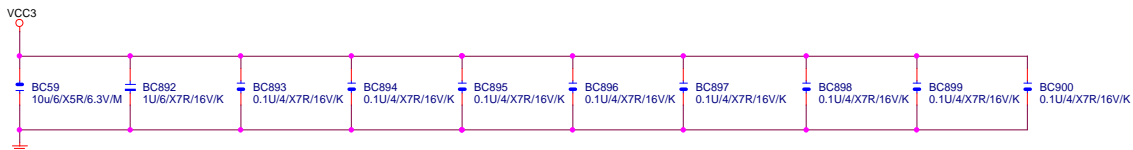
#### DFT\_GPIO0: STRAP\_DEBUG\_BUS\_PCIE\_ENABLEb

Enables the Test Debug Bus using PCIE bus  
1 : Disable ( Can still be enabled using nbcfg register access )  
0 : Enable

**GIGABYTE**™

Title		RD990 CLOCK & SYSB I/F	
Size	Document Number	Rev	
Custom	GA-990FXA-UD3	3.02	
Date:	Thursday, November 15, 2012	Sheet	11 of 35

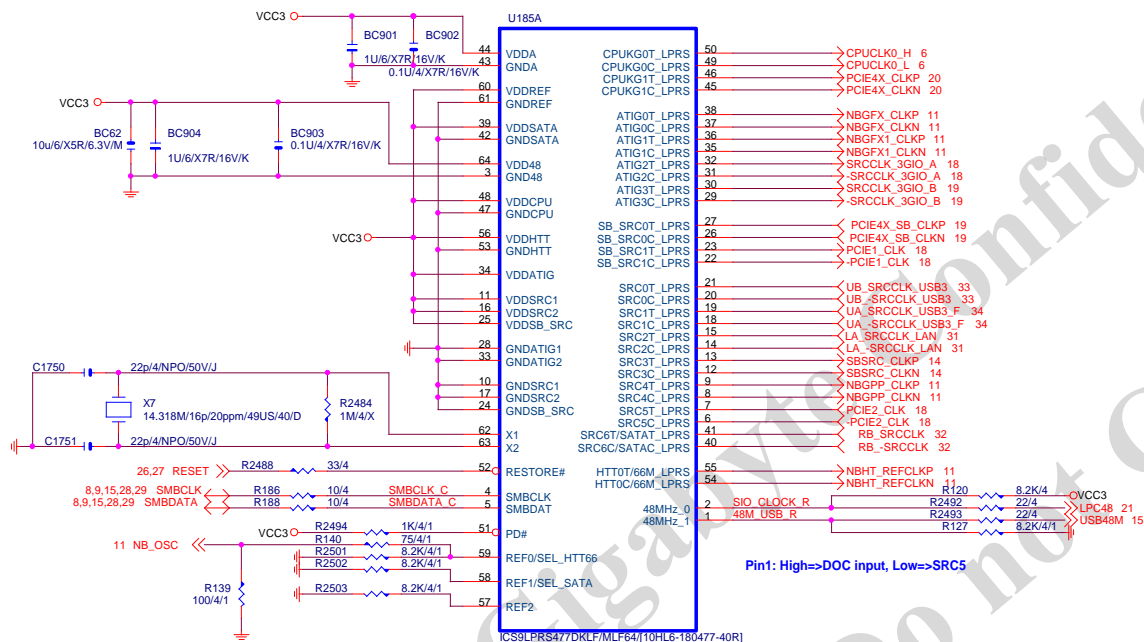




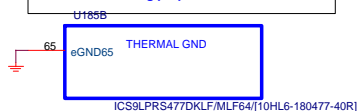
NB CLOCK INPUT TABLE

NB CLOCKS	RS740	RX780	RS780
HT_REFCLKP	66M SE(SE)	100M DIFF	100M DIFF
HT_REFCLKN	NC	100M DIFF	100M DIFF
REFCLK_P	14M SE (3.3V)	14M SE (1.8V)	14M SE (1.1V)
REFCLK_N	NC	NC	vref
GFX_REFCLK*	100M DIFF	100M DIFF	100M DIFF
GPP_REFCLK	NC	100M DIFF	100M DIFF(OUT)
GPSPB_REFCLK	100M DIFF	100M DIFF	100M DIFF

\* the GFX\_REFCLK input is required for all cases



Clock chip has internal serial terminations for differential pairs, external resistors are reserved for debug purpose.



	OSC_14M_NB
RS740	3.3V 33R serial
RX780	1.8V 82.5R/130R
RS780 (Single-ended)	1.1V 158R/90.9R

REF0/SEL_HTT66	HTT CLOCK
0	100.00 DIFFERENTIAL
1	66.66 SINGLE END

REF1/SEL_SATA	SRC6/SATA
0	100.00 DIFFERENTIAL SPREADING SRC CLOCK
1	100.00 NON-SPREADING DIFFERENTIAL SATA CLOCK

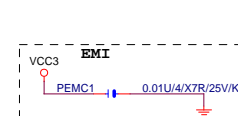
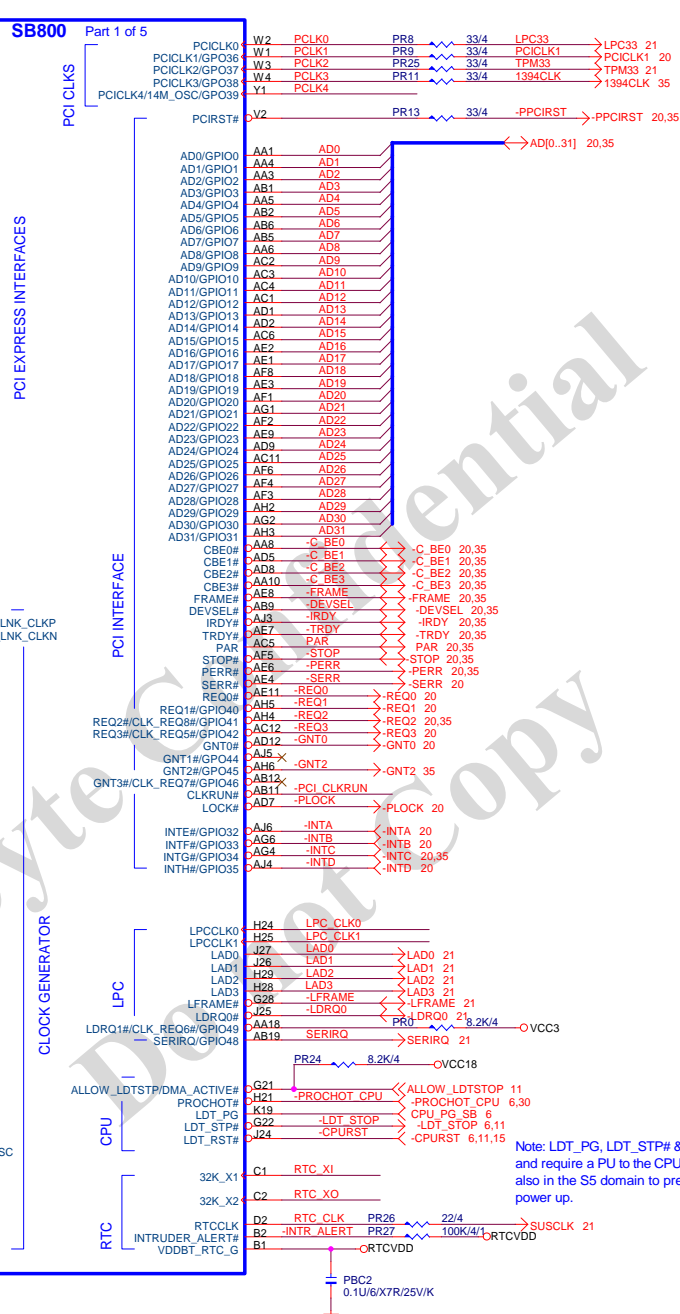
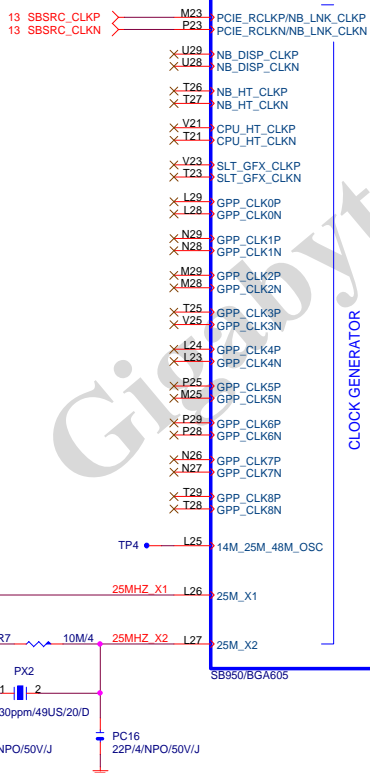
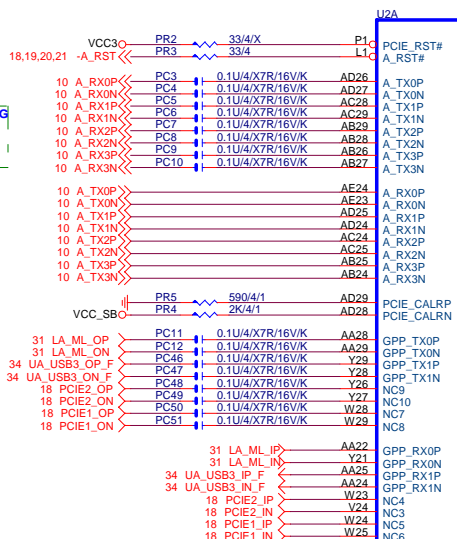
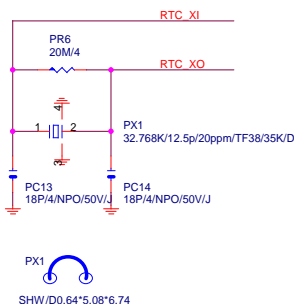
**GIGABYTE**

Title		
ICS9LPRS477		
Size	Document Number	Rev
Custom	GA-990FXA-UD3	3.02
Date:	Thursday, November 15, 2012	Sheet 13 of 35

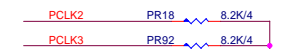


A diagram showing a square with a vertical line segment extending upwards from the top-left corner. This segment is labeled  $SB_{HS}$  and has a red 'X' at its top end.

SB\_HS/[12SP2-S06510-11R\_12SP2-S06510-12R\_12SP2-S06510-13R]



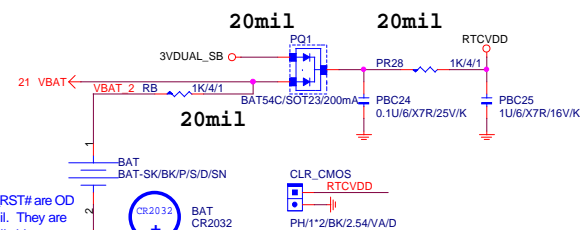
Low: Force PCIe GEN1, Up: Allow PCIe GEN2



	PCLK2	PCLK3
PULL HIGH	WATCHDOG TIMER ON NB_PWRGD ENABLED	USE DEBUG STRAPS
PULL LOW	WATCHDOG TIMER ON NB_PWRGD DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT

BIOS after boot setting  
EC AOD-ACC

LPC_CLK0 Rev.A12	LPC_CLK1
IMC ENABLED	CLKGEN ENABLED
AOD Extreme IMC DISABLED	CLKGEN DISABLED
DEFAULT	DEFAULT



CLR_CMOS	
SHORT	CLEAR CMOS
OPEN	NORMAL

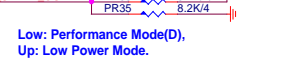
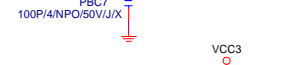
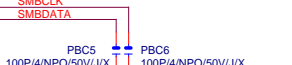
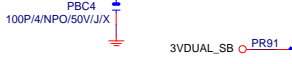
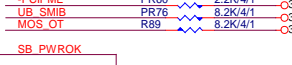
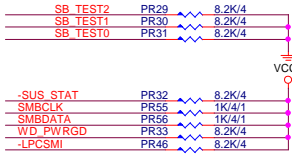
**NOT ADD ICT FOR RTCVDD PIN**

**GIGABYTE**

Title	ATI SB950 PCIE/PCI/CPU/LPC
-------	----------------------------

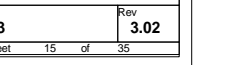
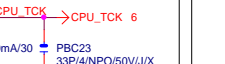
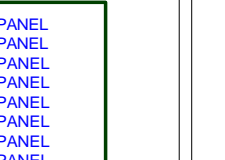
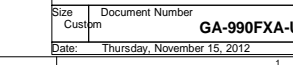
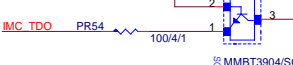
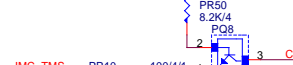
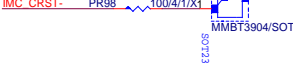
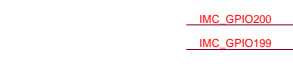
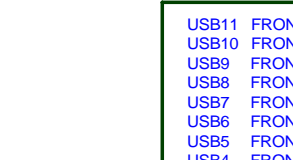
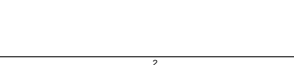
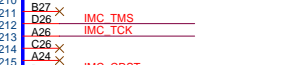
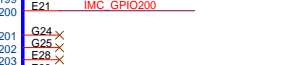
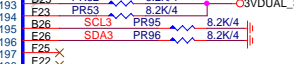
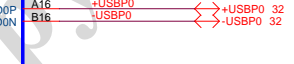
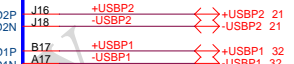
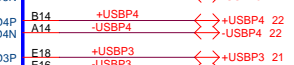
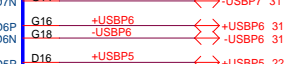
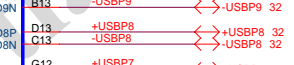
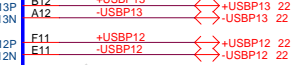
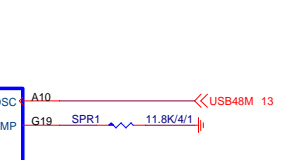
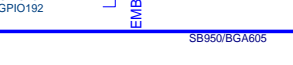
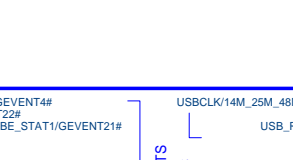
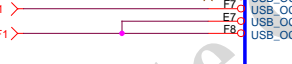
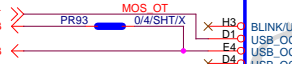
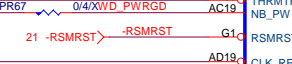
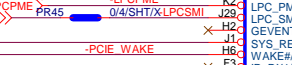
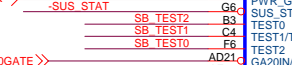
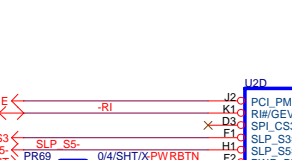
Size Custom	Document Number <b>GA-990FXA-UD3</b>	Rev <b>3.02</b>
Date: Thursday, November 15, 2012	Sheet 14 of 35	





Low: Performance Mode(D),  
Up: Low Power Mode.

Low: Disable PCI MEM boot(D),  
Up: Enable PCI MEM boot

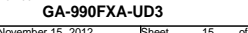
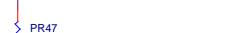
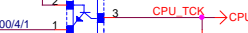
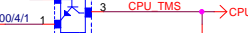
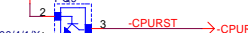


USB11	FRONT PANEL
USB10	FRONT PANEL
USB9	FRONT PANEL
USB8	FRONT PANEL
USB7	FRONT PANEL
USB6	FRONT PANEL
USB5	FRONT PANEL
USB4	FRONT PANEL
USB3	REAR PANEL
USB2	REAR PANEL
USB1	REAR PANEL
USB0	REAR PANEL

either HWM inputs or PWR\_GD signals  
can be used for power-up sequencer

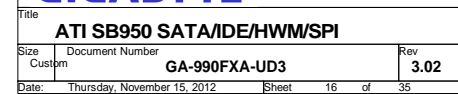


ROM TYPE:  
H, H = Reserved  
L, L = SPI ROM DEFAULT  
L, H = LPC ROM  
L, L = FWH ROM



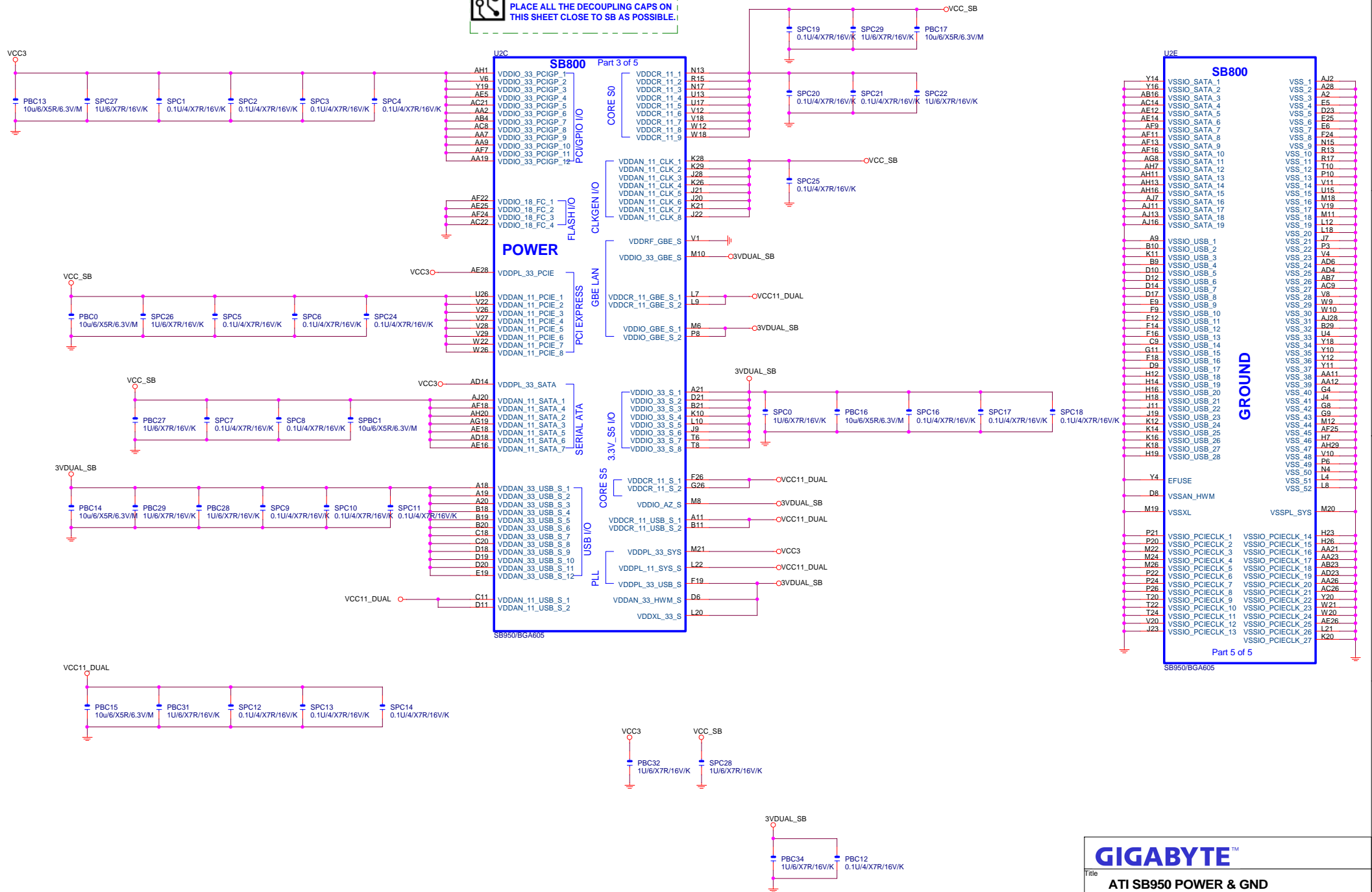
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Title ATI SB950 ACPI/USB/GPIO/AUDIO		
Size Custom	Document Number GA-990FXA-UD3	Rev 3.02
Date: Thursday, November 15, 2012	Sheet 15	of 35







PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB AS POSSIBLE.



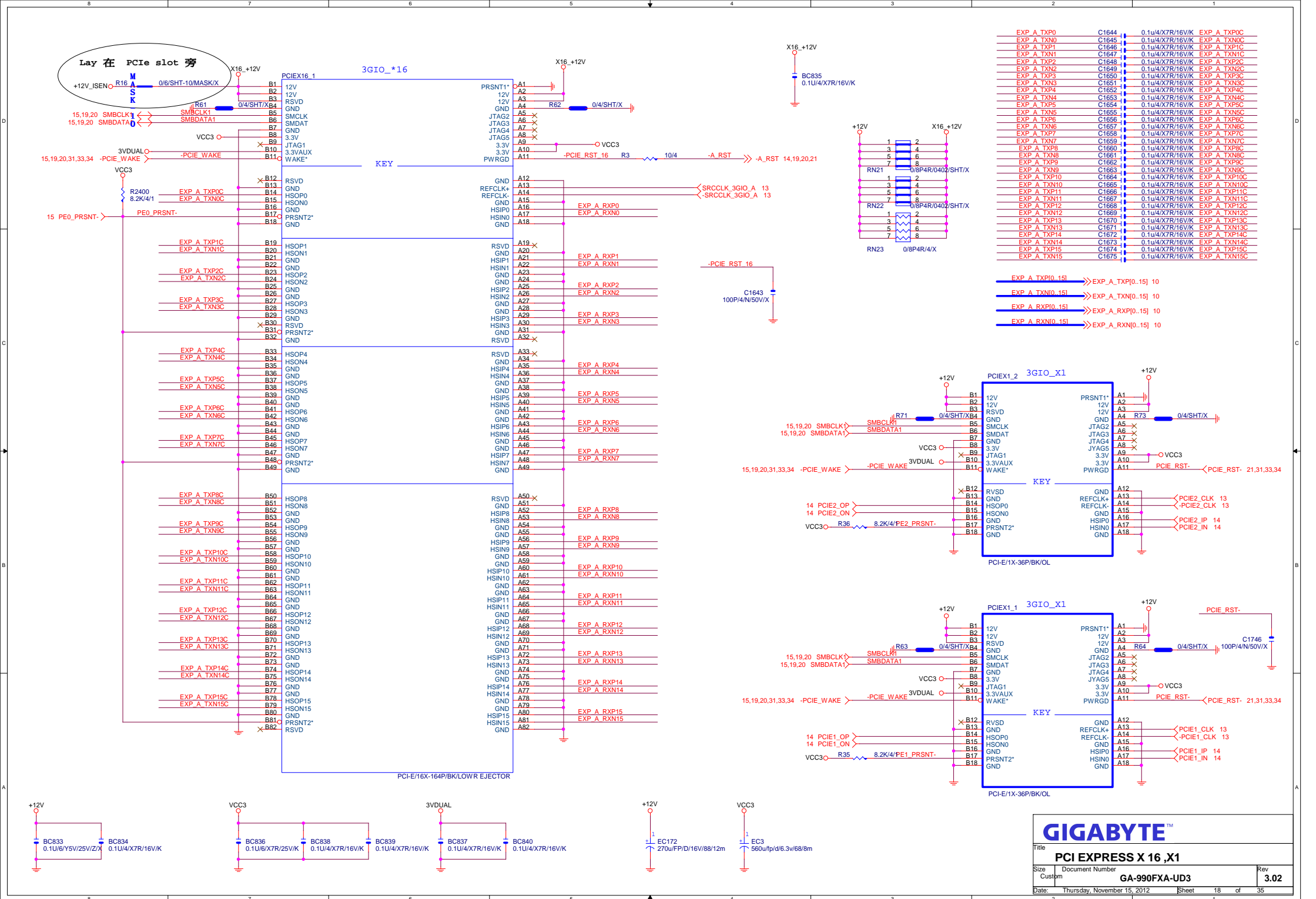
**GIGABYTE™**

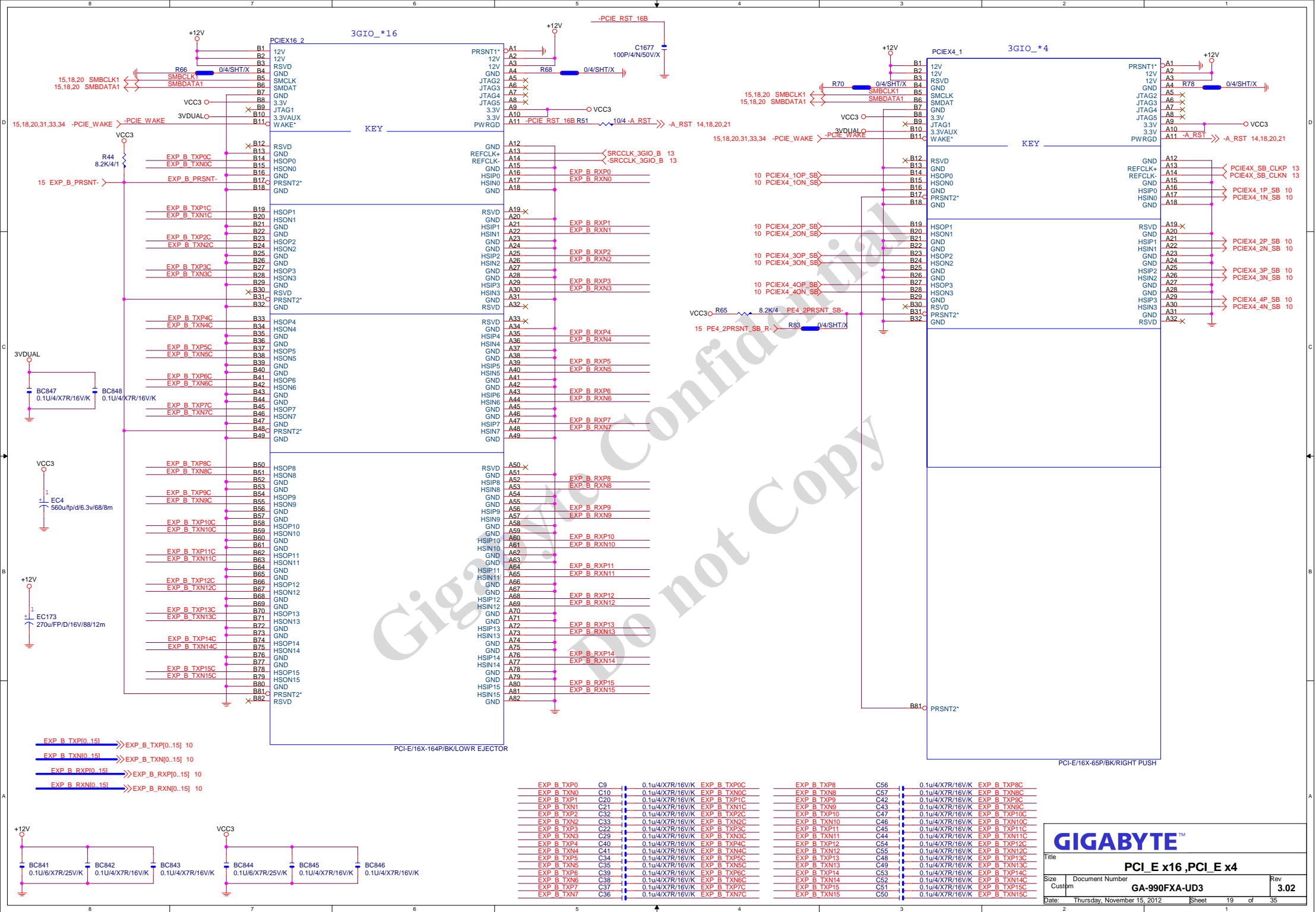
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**ATI SB950 POWER & GND**

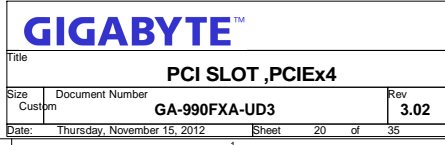
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Document Number  
**GA-990FXA-UD3**

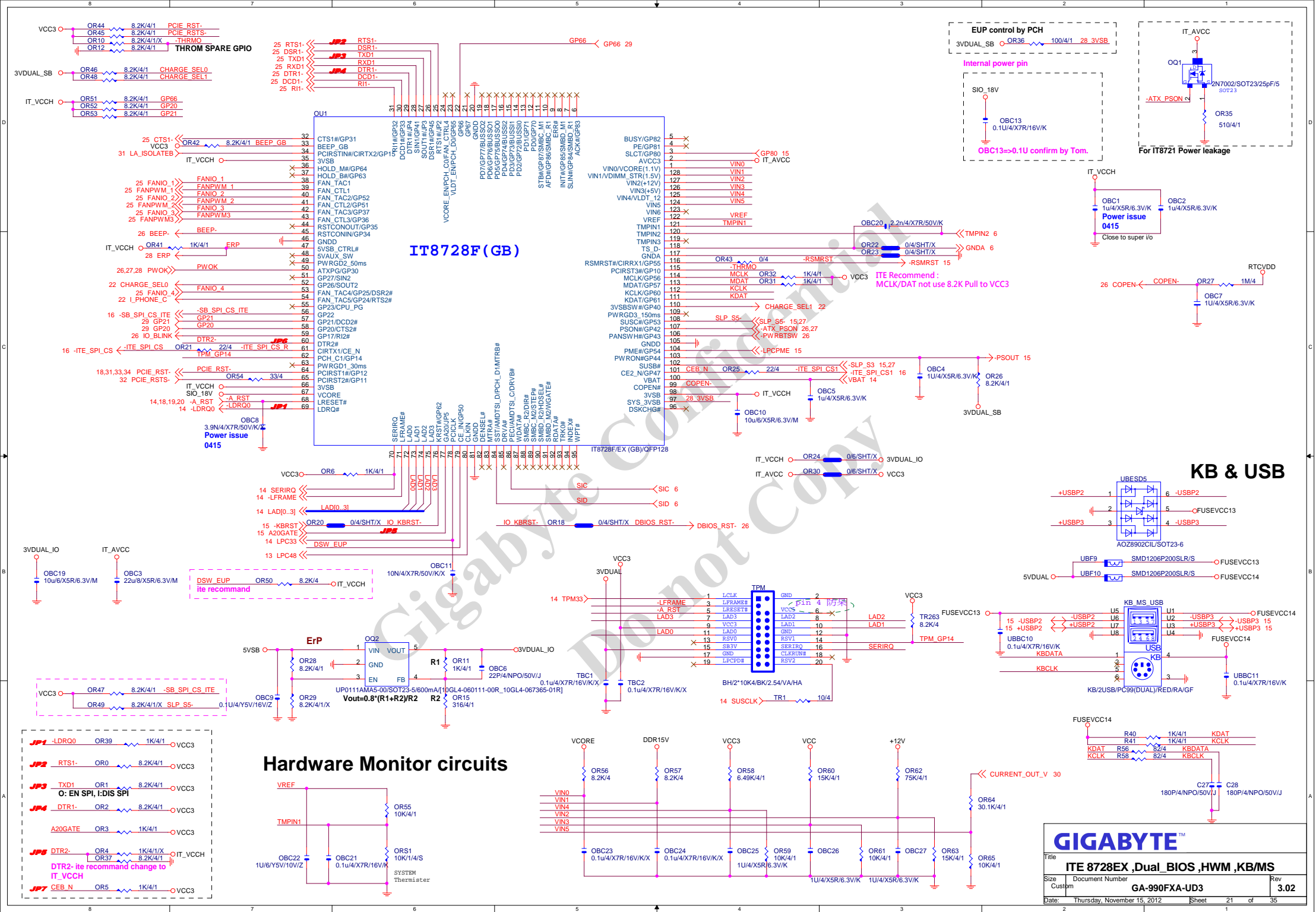
Rev  
**3.02**

Date: Thursday, November 15, 2012 Sheet 17 of 35









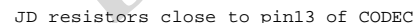






ALC889/VT2021 Colay

co-layout



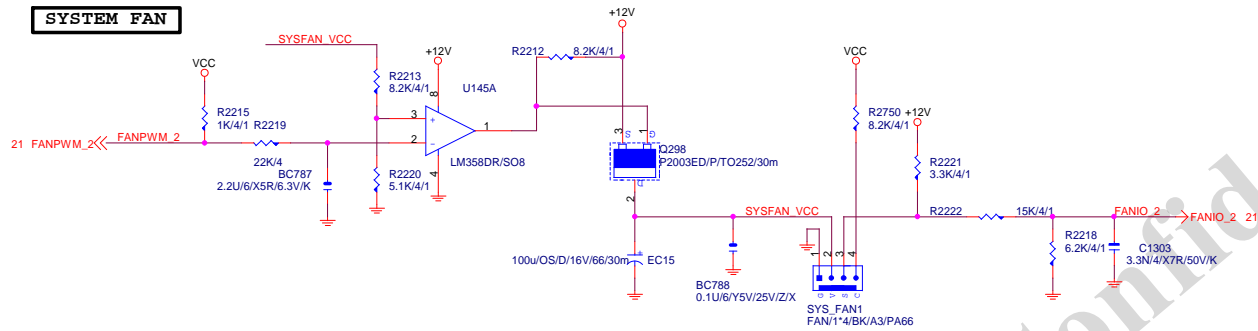
## Gigabyte Technology

HD AUDIO ALC889A

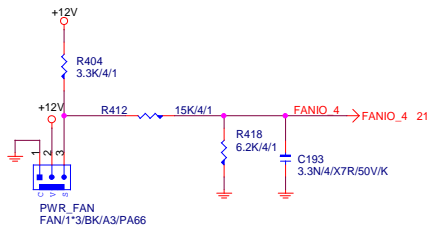
Size Custom	Document Number <b>GA-990FXA-UD3</b>	Rev <b>3.02</b>
Date:	Thursday, November 15, 2012	Sheet 23 of 35



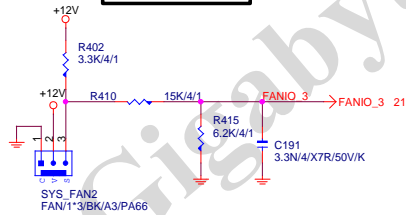
# SYSTEM FAN



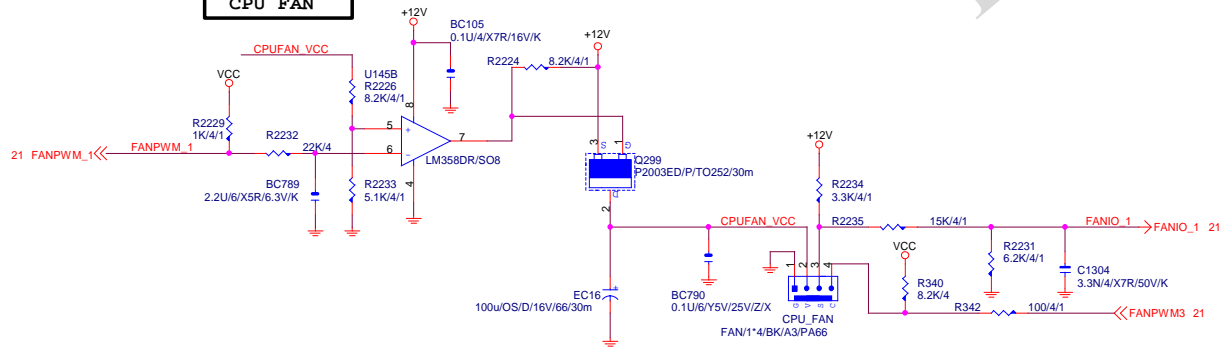
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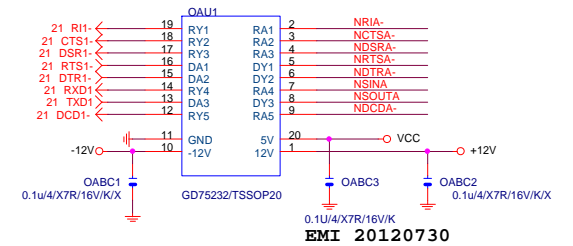
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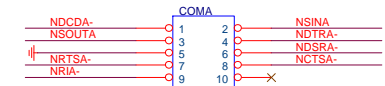
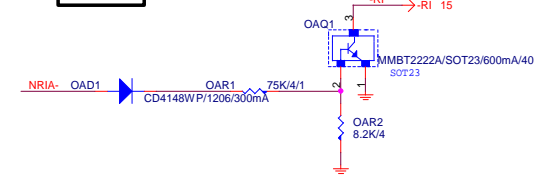
# CPU FAN



# COMA

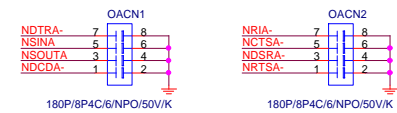


# COM RI



BH25K10/BK/2.54VA/COM

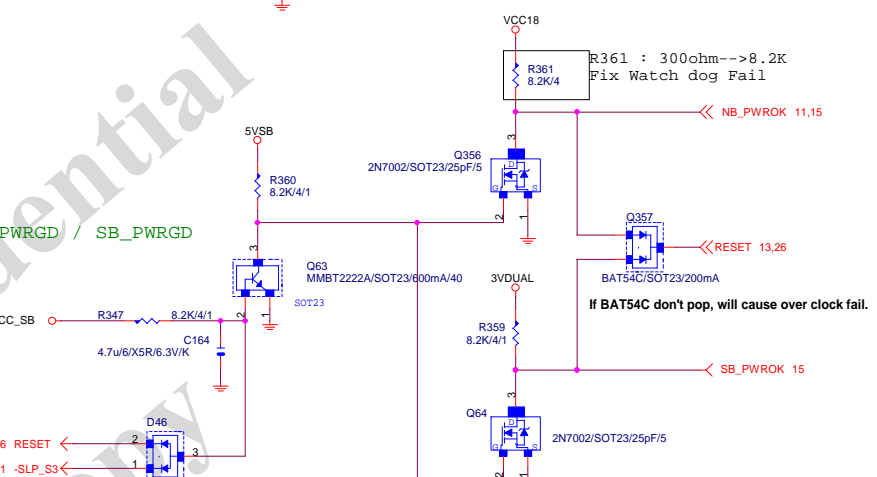
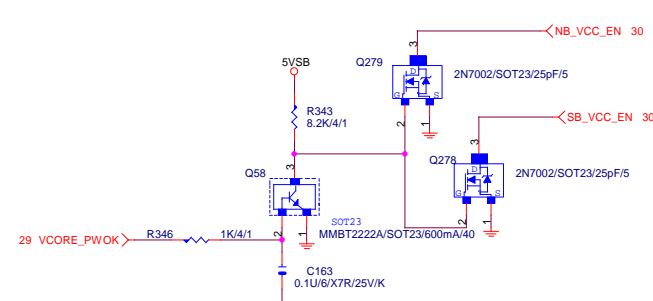
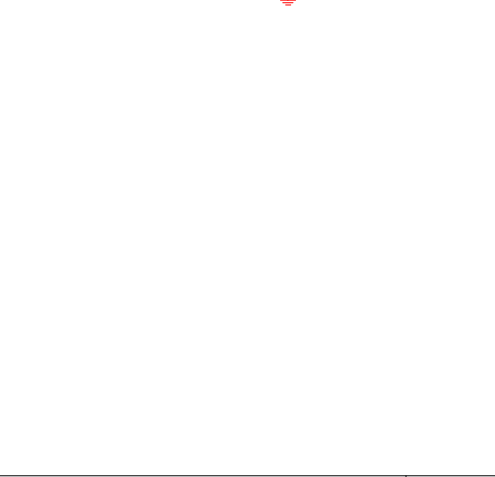
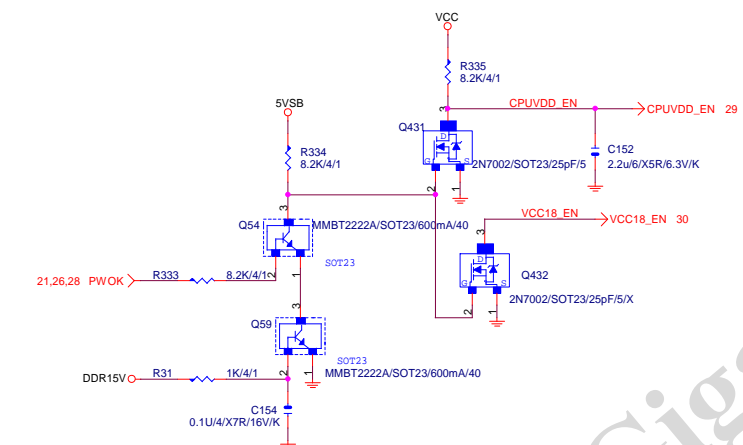
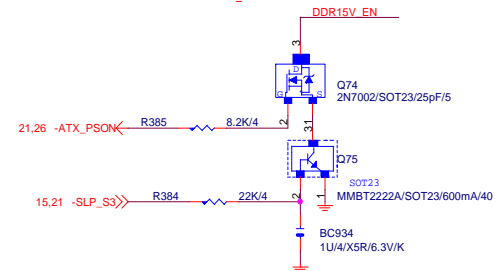
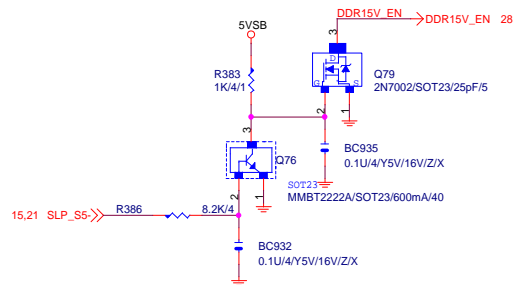
11NH3-000205-Y1R/Y2R



**GIGABYTE**

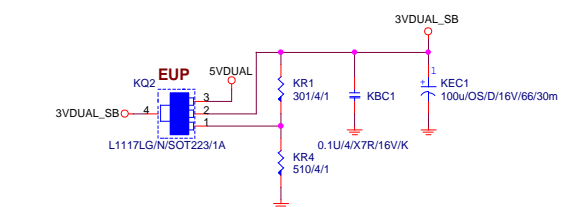
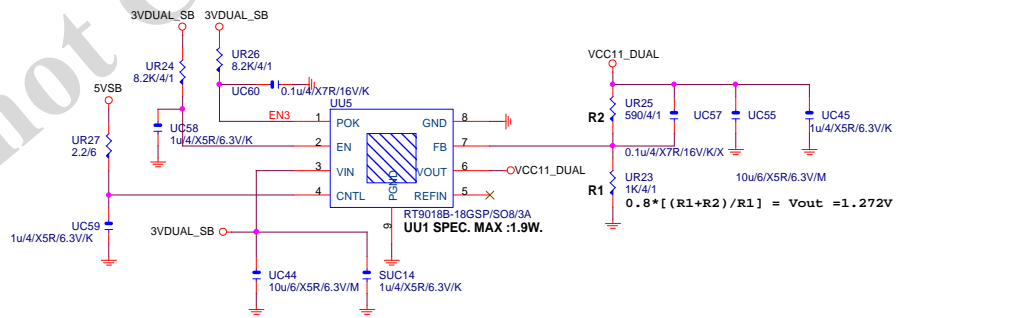
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Size	Document Number	Rev	3.02
Custom	GA-990FXA-UD3		
Date:	Thursday, November 15, 2012	Sheet	25 of 35



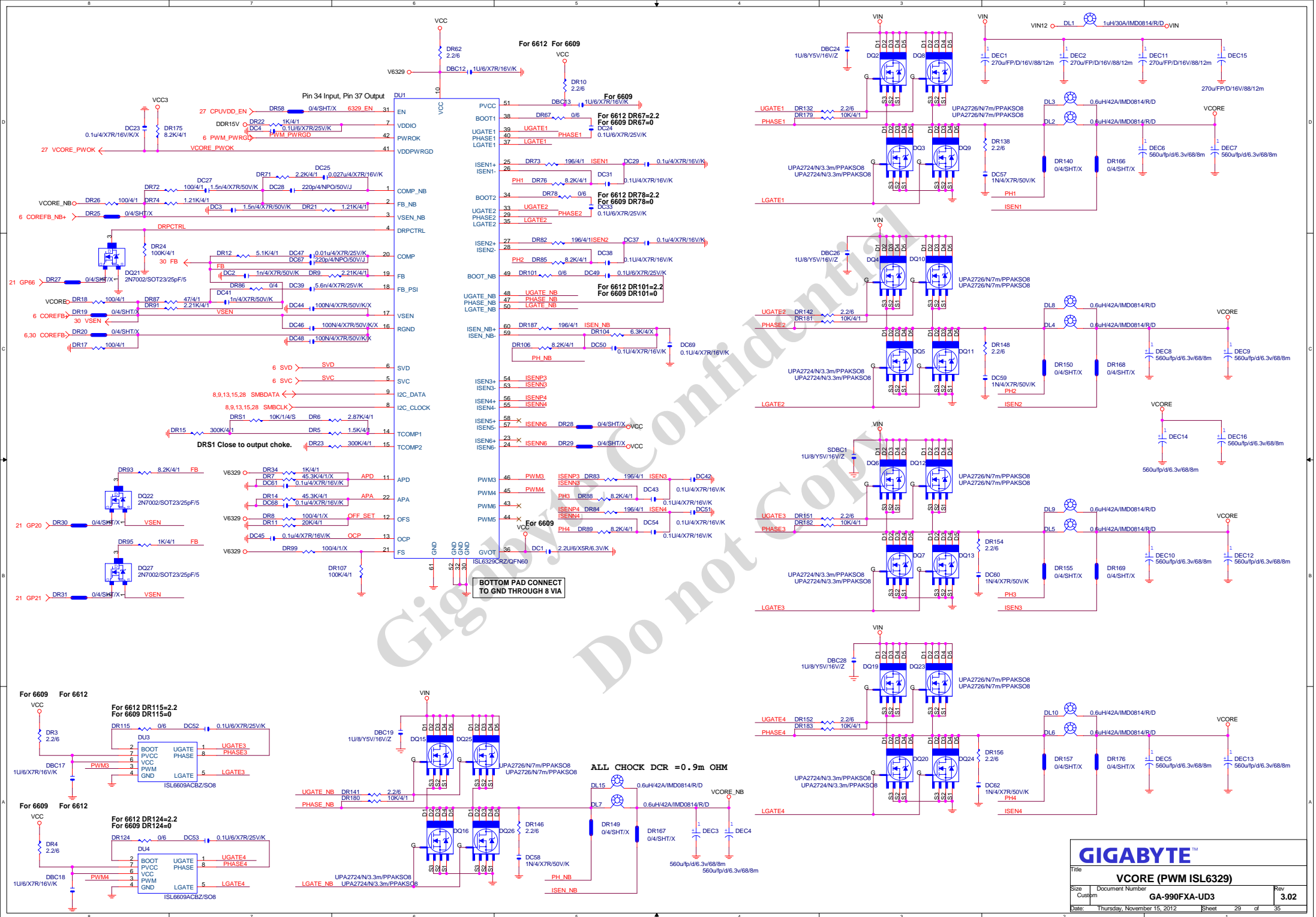


PWOK > NB\_PWRGD / SB\_PWRGD

( 1.8V , 1.2V , 1.1V ) > NB\_PWRGD 前 1ms



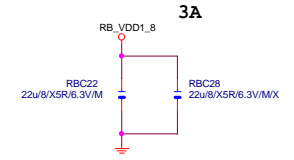
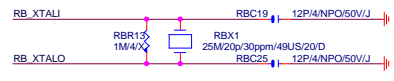
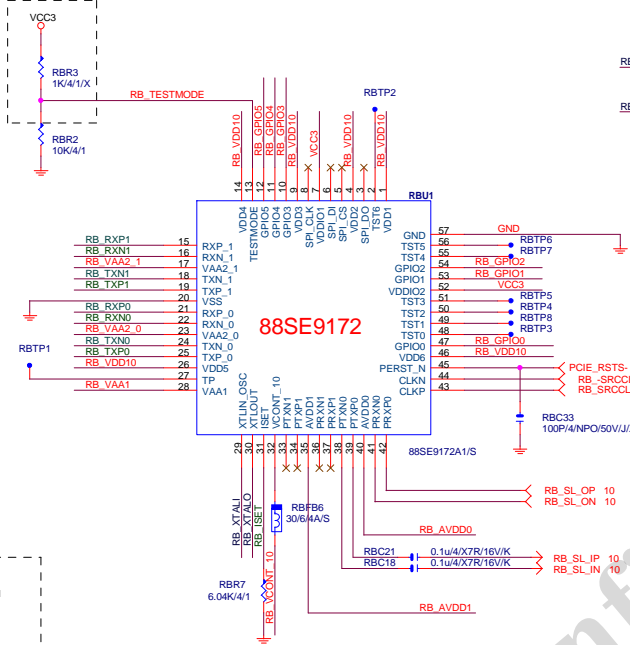
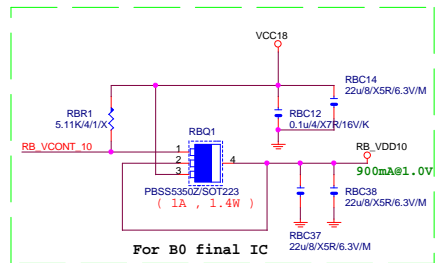
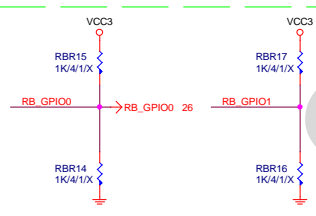
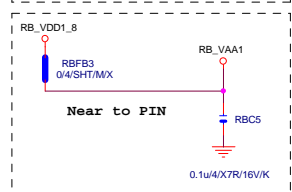
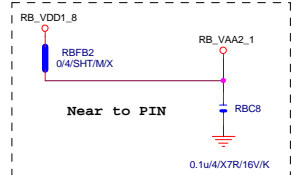
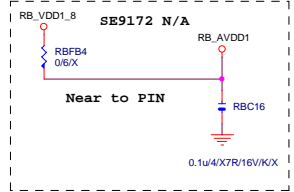
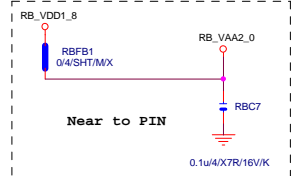
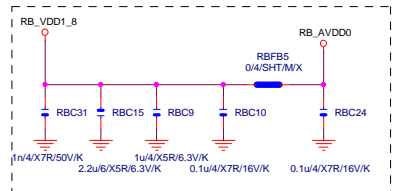
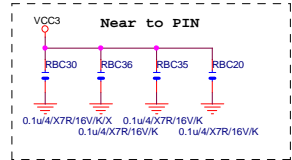
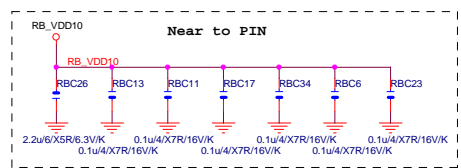




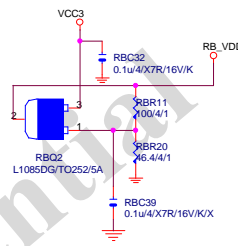




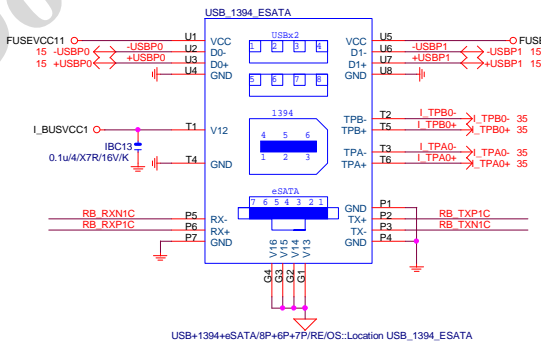
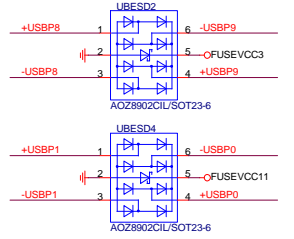
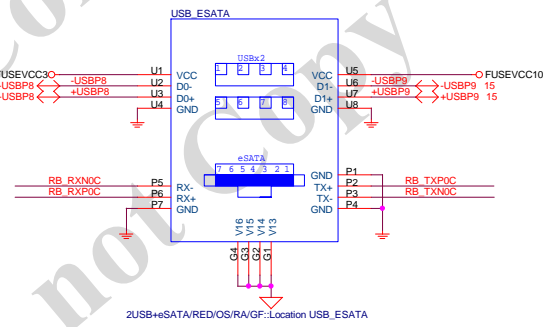
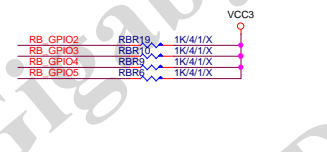
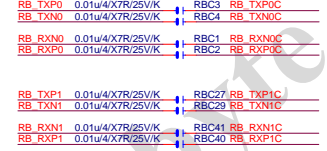


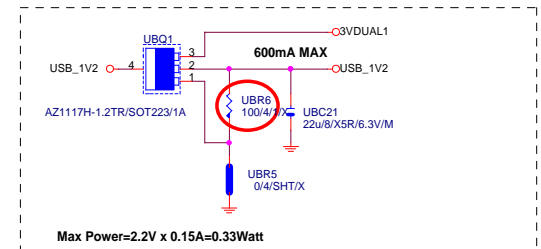
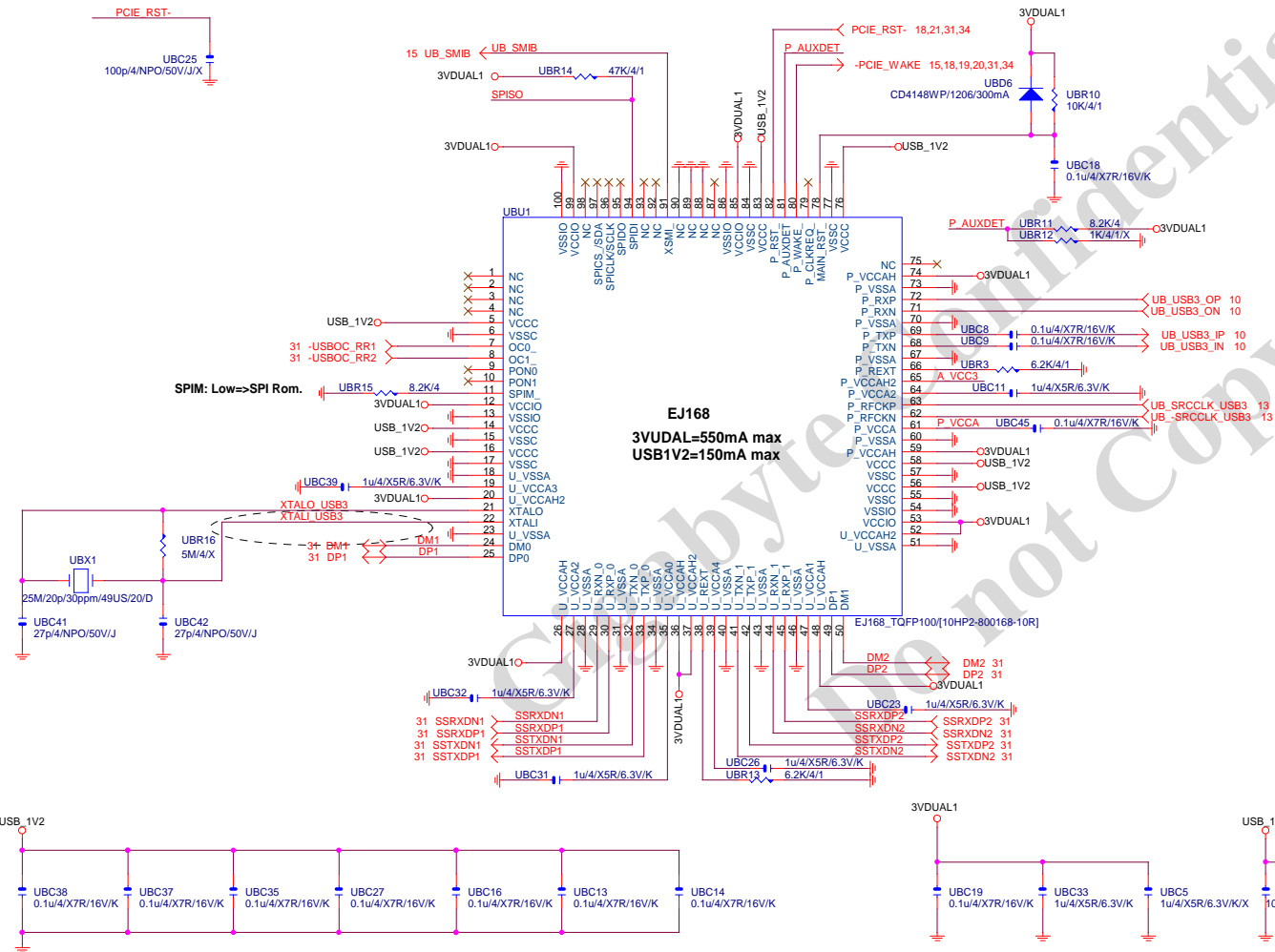
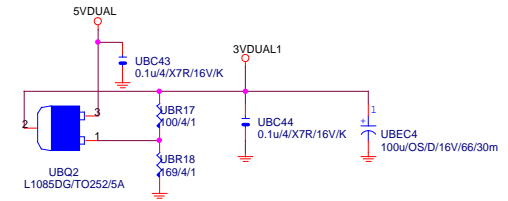
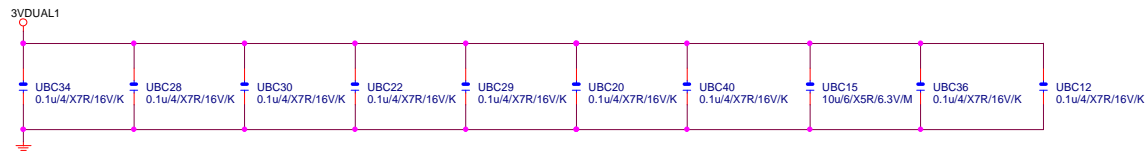


### 3.3V to 1.8V Voltage Regulator



900mA: [20/4.5/7.5/4.5/20]





AZ1117H-1.2TR/SOT223/1A-->UR17:0/4,UR16:N/A [1.2V]

L1117LG/N/SOT223/1A-->UR17:0/4,UR16:100/4/1 [1.25V]

USB3.0 --> 5GHz  
BANDWIDTH=5GHz\*(8b/10b)=4Gb/s=500MB/s

GIGABYTE™			
Title	EJ168 R_USB30		
Size	Document Number	Rev	
Custom	GA-990FXA-UD3	3.02	
Date:	Thursday, November 15, 2012	Sheet	33 of 35



